REMARKS

In the Office Action dated August 11, 2004, claims 1, 2, 4-12, 14-21, and 34-36 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,678,026 (Vartti) in view of U.S. Patent No. 5,740,401 (Hanawa); and claims 3 and 13 were rejected under § 103 over Vartti in view of Hanawa, and U.S. Patent No. 6,092,156 (Schibinger). Applicant acknowledges the indication that claims 22-33 contain allowable subject matter. Claim 22 has been amended from dependent form to independent form, with its scope *unchanged*, to place the claim in condition for allowance. The only change made to claim 22 is to form, with "process bus" changed to "processor bus" at lines 4 and 21.

As amended, claim 1 is allowable over the asserted combination of Vartti and Hanawa. Claim 1 now recites: requesting exclusive access to a first memory location of a shared memory by a first processor; granting exclusive access to the first memory location of the shared memory to the first processor; allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location; and storing access request information associated with the exclusive access in a first register in a first memory controller *and* in a second register in a second memory controller. Neither Vartti nor Hanawa teaches or suggests storing of access request information associated with an exclusive access in registers of both first and second memory controllers.

Although Vartti shows two storage controllers 1 and 2 (see Figure 1 of Vartti), there is no indication or suggestion that the lock request information associated with a lock request is stored in both the first and second storage controllers. In fact, the lock request information is stored only in the storage controller associated with the memory subsystem that the request is targeted for.

Similarly, in Hanawa, there is no indication or suggestion that access request information associated with an exclusive access is stored in two different memory controllers – the access queue depicted in Figure 1 of Hanawa is designed to store the access request information associated with an access request of a particular memory bank 130 or 140 – there is no need in Hanawa of storing access request information in different memory controllers.

Thus, even if Vartti and Hanawa can be properly combined, the hypothetical combination of Vartti and Hanawa would not teach or suggest all elements of claim 1. Therefore, a *prima facie* case of obviousness of claim 1 cannot be established over the asserted combination of Vartti and Hanawa. *See* M.P.E.P. § 2143 (8th ed., Rev. 2), at 2100-129.

Newly added independent claim 41 is allowable over the asserted combination of Vartti and Hanawa because the hypothetical combination of these references would not teach or suggest the multiprocessor system having a plurality of multiprocessor nodes, where each of the multiprocessor nodes comprises a shared memory, a processor to request exclusive access of a memory location in the shared memory, and a memory controller to forward access request information associated with the exclusive access from the multiprocessor node for storage of the access request in another multiprocessor node; and a switch to receive the access request information and to send the access request information to the multiprocessor nodes for storage of the access request information in respective registers of the memory controllers.

Claim 34 has been amended from dependent form to independent form, with the scope of the claim remaining *unchanged.* Claim 34 recites that requesting exclusive access includes sending a lock request from a first processor to a first memory controller coupled to a shared memory, forwarding the lock request from the memory controller to a switch, and the switch broadcasting lock request information to the first memory controller and *at least another memory controller.* The Office Action rejected claim 34 by referencing the rejections of claims 2 and 4. Note that claims 2 and 4 do not recite the same subject matter as claim 34. Specifically, claims 2 and 4 do not recite a switch broadcasting lock request information to a first memory controller and at least another memory controller. Neither Vartti nor Hanawa teaches such a switch for broadcasting lock request information to multiple memory controllers. Therefore, the hypothetical combination of Vartti and Hanawa does not teach or suggest the claimed invention. A *prima facie* case of obviousness has thus not been established with respect to claim 34.

Independent claim 10, as amended, is allowable because the asserted combination of Vartti and Hanawa does not teach or suggest requesting exclusive access to a first memory location of a shared memory of a *first* multiprocessor node by a first processor

of the first multiprocessor node, and sending, by a switch, access request information associated with the exclusive access of the shared memory of the *first* multiprocessor node to a *second* multiprocessor node. In Vartti and Hanawa, a request that is targeted for a particular memory subsystem is processed by the associated memory controller or storage controller – there is no teaching or suggestion in either Vartti or Hanawa of a first memory or storage controller sending access request information associated with an exclusive access in a first multiprocessor node by a switch to *another* memory or storage controller. Therefore, a *prima facie* case of obviousness cannot be established with respect to claim 10 over the asserted combination of Vartti and Hanawa.

Dependent claims, including newly added dependent claims 38-40 and 42, are allowable for at least the same reasons as corresponding independent claims. Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees, including extension of time fees, and/or credit any overpayment to Deposit Account No. 08-2025 (200301872-1).

Respectfully submitted,

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